Ka band power pHEMT technology for space power flip-chip assembly

E. ROGEAUX[(1)], J-P. FRAYSSE[(1)], C. SCHAFFAUSER[(1)], S.GEORGE[(1)],
D. PONS[(2)], P. FELLON[(2)], D. GEIGER[(2)], D. THERON[(3)], N. HAESE[(3)], S. VERDEYME[(4)],
R. QUERE[(4)], D. BAILLARGEAT[(4)], E. NGOYA[(4)], S. LONG[(5)], L. ESCOTTE[(5)]

[(1)]Alcatel Space Industries, 26 Av JF.Champollion, 31037 Toulouse Cedex, France
[(2)]United Monolithic Semiconductors, 91401 Orsay Cedex France
[(3)]Institut d'Electronique et Microélectronique du Nord, 59652 Villeneuve d'Ascq Cedex, France
[(4)]Institut de Recherche en Communications Optiques et Micro-ondes, 87060 Limoges Cedex, France
[(5)]Laboratoire d'Analyse et d'Architecture des Systèmes, 31077 TOULOUSE Cedex, France

***Abstract* — This paper proposes a released power pHEMT process for flip-chip mounting. The potential of this flip-chip process is demonstrated for power and low-noise applications in Ka-band.**

I. INTRODUCTION

Flip-chip technology (FC) is a promising candidate for the use in a new generation of broadband multimedia satellites where thermal management and miniaturisation are key enabling criterias. Applying flip-chip technology to high power GaAs devices (HBTs and pHEMTs) have been demonstrated by several Research Institutes and company's over the last few years with impressive results [1-5].

In this paper, we presented the work done inside the "Optimal" project (RNRT project) to adapt the power pHEMT process PPH25 from United Monolithic Semiconductors for the use of flip-chip assembly. Both the power performance and the low-noise performance of this process will be evaluated. This allows the fabrication of high-power and low-noise MMICs in one wafer run. An optimized layout of the flip-chip transistor cell shows a reduction of the thermal resistance compared to the standard configuration. A 3-D electromagnetic analysis, a non-linear electro-thermal model and a noise model will be presented. Thus all elements for the design of low-noise and high-power MMICs will be available.

II. TECHNOLOGY DEVELOPMENT

The work is based on the PPH25 process (0.25µm power-pHEMT) of United Monolithic Semiconductors. In order to reduce the channel temperature of the transistors, 3-D simulations have been performed using the finite element method. As border conditions we took a temperature of 55 °C for the heat sink and a worst case approximation for the power dissipation of 1.2W/mm. A conventional structure (up-side up mounting, 100 µm substrate thickness with via-holes) was calculated for the assessment and comparison of the different bump-configurations Fig.1.

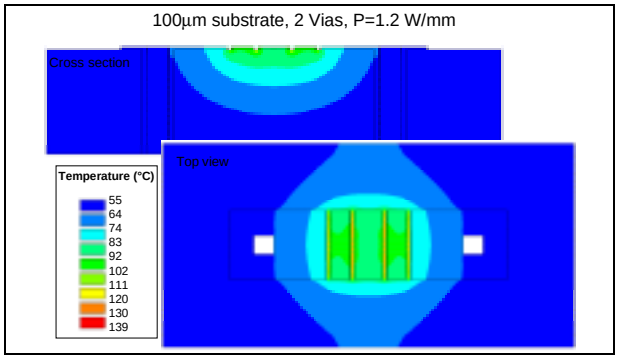

Fig.1 : Thermal calculation of the conventional structure with 100µm substrate thickness an up-side up mounting.

With the conventional configuration a maximum channel temperature of 139°C is obtained. This result was compared to different flip-chip configurations. From this calculations we found that it is absolutely necessary to implement a thermal bump on each source pad. The results of the thermal calculations using a optimized bump configuration is shown in Fig.2.

With the optimized configuration we found a maximum channel temperature of 118 °C, which is indeed 21 °C lower as compared with conventional mounting.

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This demonstrates the potential of the flip-chip mounting for high power applications.

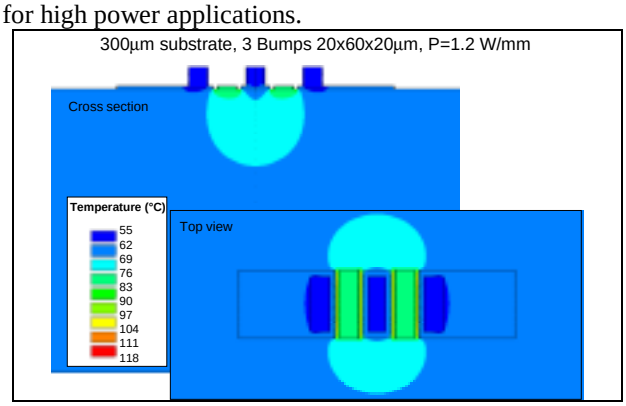

Fig.2 : Thermal calculation of a flip-chip configuration with thermal bumps on each source pad.

The next step was the development of an appropriate bump technology. To avoid coupling between the CPW chip and the substrate a bump height of 30 µm has to be realized. However the lateral size of the thermal bumps is limited as an increase of the transistor size leads to a degradation of the RF-performance. Taking this into account a lateral size of 20 µm for the thermal bumps seems to be a good compromise between the RF-performance on the one hand and the technological difficulties as well as the thermal resistance on the other hand. A difficulty was to realize air-bridges and bump on the same transistor to have the possibility for on-wafer testing.

By implementing a probimid resist system and controlling the electroplating conditions, we succeed in the development of smooth bumps which are compliant with the above mentioned demands. The Au-bumps show a smooth surface and no porosity. Thus the bumps are well suited for the use of thermo compression mounting. The choice to use Au-bumps and consequently thermo compression mounting is due to the fact, that the Au-bumps show a superior thermal behavior compared to solder bumps Fig.3.

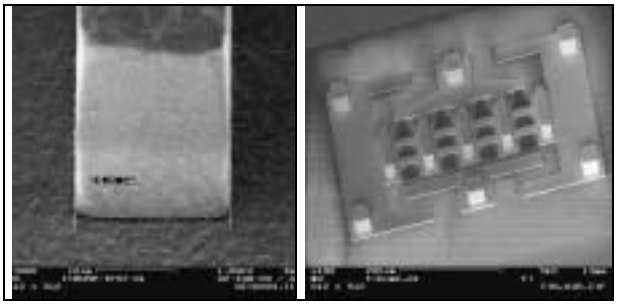

Fig.3 : Detail view of a rectangular bump and a multifinger transistor with thermal bumps on each source pad. :

An electrical comparison of PPH25 standard transistors and transistors with thermal bumps on each source pad has been performed to evaluate the impact of increased source pad size. As shown in Fig.4 , the effects are negligible up to 34 GHz.

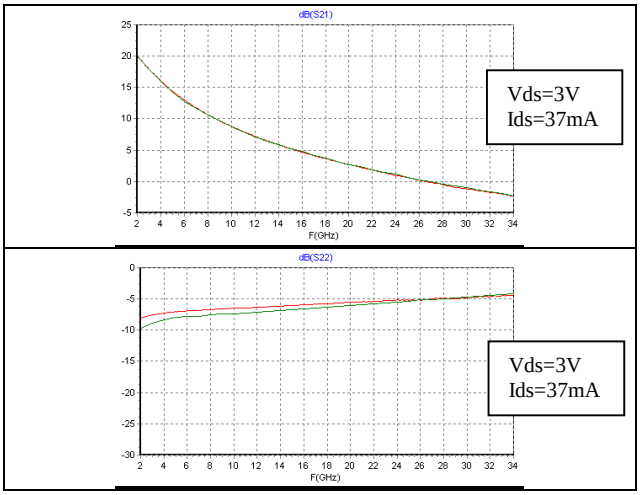

Fig.4 : Transistors with and without bumps

III. FLIP-CHIP MOUNTING EFFECTS

The coplanar technology is well suited for flip-chip mounting. So the second topic studied in the project was to define the impacts of parasitic effects of the flip-chip transitions. First the effects of a substrate over coplanar lines was investigated. Then the transistors with thermal bumps have been specially addressed (Fig.5).

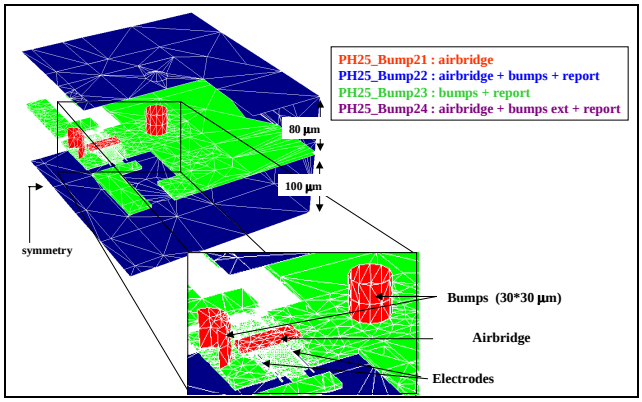

Fig.5 : 3-D bumped transistors.

3-D simulations were performed applying an hybrid approach combining a Finite Element software developed at the IRCOM and a circuit one [6]. The results showed very little impact of carrier substrate on the transistor behavior up to 30 GHz as showed on Fig.6.

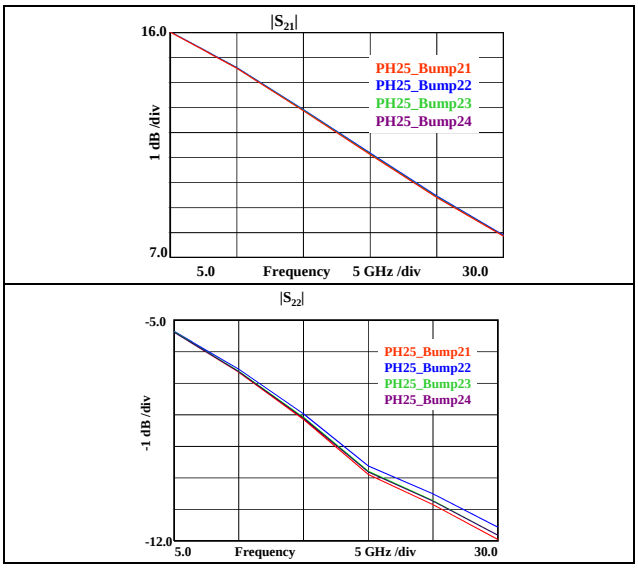

Fig.6 : 3-D-electromagnetic simulations of the flip-chip mounted transistors.

These simulated results have been validated by experiments: chips have been mounted on 635µm thick Alumina carriers and S-parameter measurements up to 34GHz have been carried out before and after the flip-chip mounting (Fig.7). The transistors showed a nearly identical behavior before and after the flip-chip mounting.

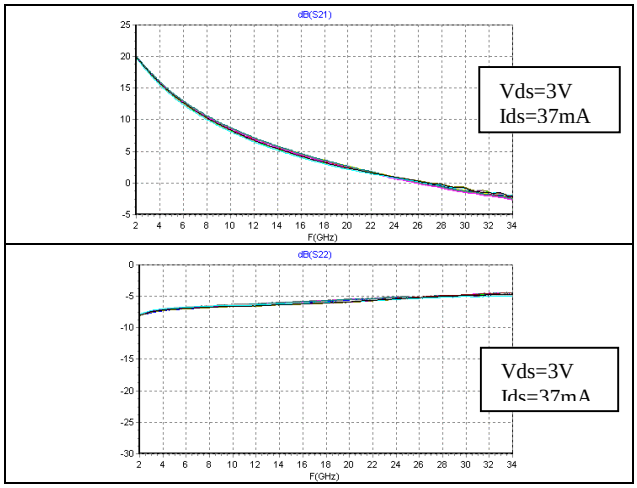

Fig.7 : S-parameters before and after flip-chip mounting

IV. Electro-thermal Non linear and noise modeling

Electro-thermal non linear modeling

An electro-thermal model has been performed taking into account the bumps and thermal resistance of the transistors (Fig.8).

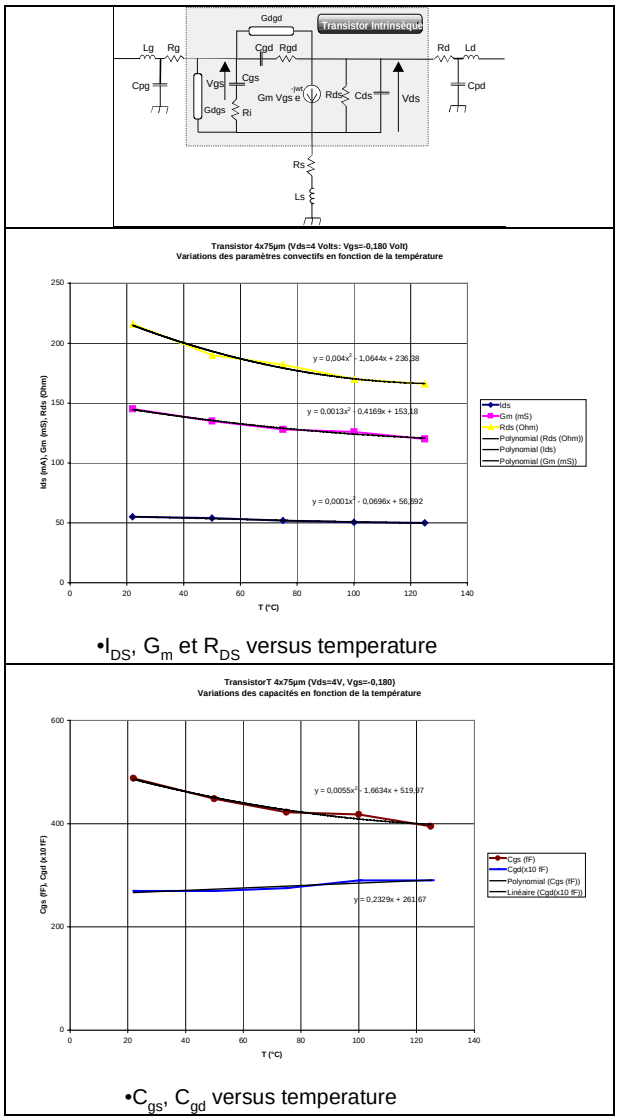

Fig.8 : Electro-thermal modeling of a 4x75µm transistor

CW mode and multi-tone simulations have been performed on 4x75µm and 8x75µm transistors. The optimum load impedances have been determined for the HPA design in K band to assume a NPR (Noise to Power Ratio) greater than 16 dB (Fig.9).

	Zload	PAE	POUT	GAIN
4x75µm	35+j35ohm	≥44%	≥19dBm	≥11dB
8x75µm	16+j18ohm	≥34%	≥20dBm	≥ 8 dB

Fig.9 : Optimum load impedance (NPR>16dB)

Noise modeling

Despite the usage of a power process, the noise performance of the PPH25 process has been determined to allow the fabrication of LNAs and HPAs in one wafer run.

The use of the PPH25 process for low-noise applications at Ka-band is still reasonable as this process offers high gain and low capacities at this frequencies. In Fig.10 the results of the noise modeling of the PPH25 process are compared to the UMS low noise process PH25.

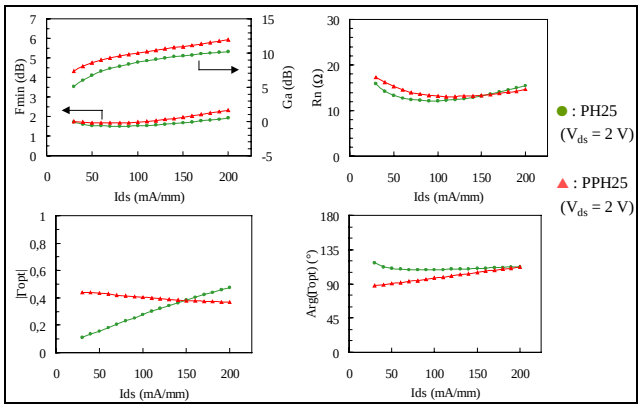

Fig.10 : PH25 and PPH25 noise parameters at 30GHz (4x30µm)

The PPH25 shows a very comparable noise behavior as the PH25 process. At 30 GHz a minimum noise figure below 2 dB and an associated gain in the range of 10 dB was found. This demonstrates that both, high power and low noise applications, could be addressed with the PPH25 process. A design of coplanar technology LNA at 30GHz based on 3 stages (6x30µm) biased at 13.5mA Vds=2V, is ongoing and previous simulation results based on CPW lines Heinrich models are given on Fig.11.

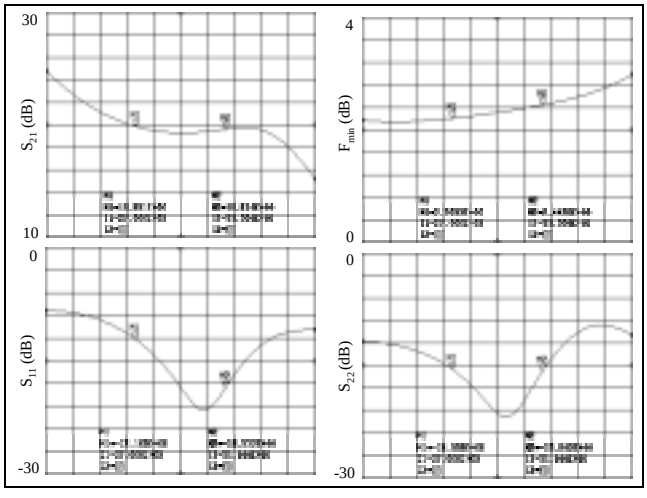

Fig.11 : LNA simulation results

V. Conclusion

The power pHEMT process (PPH25) of United Monolithic Semiconductors has been extended for the use of flip-chip mounting. Thermal calculations showed that the maximum channel temperature could be decreased with the flip-chip approach. This was possible by adding thermal bumps on each source pad. From electromagnetic simulations and from S-parameter measurements up to 34 GHz, no negative effects of the flip-chip transitions were detected. A non linear electro-thermal model has been established for CW and multi-carrier simulations. From a noise modeling we found that this process could be used both for power applications and for low-noise applications at Ka-band.

The available technology (PPH25 for flip-chip) will be further validated by the realization of CPW high-power and low noise-amplifiers at Ka-band.

ACknowledgement

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